CLAIMS

The invention claimed is:

1. A method of forming an electrically insulative surface over a semiconductor substrate, comprising:

providing a substrate having a non-planar surface topography;

forming a spin-on-dielectric material over the non-planar surface topography of the substrate;

forming a second dielectric material over the spin-on-dielectric material; and

polishing the second dielectric material while using the spin-on-dielectric material as a polishing stop, the polishing utilizing conditions which remove the second dielectric material at a faster rate than the spin-on-dielectric material, the polishing forming an electrically insulative surface over the semiconductor substrate with such surface comprising both the spin-on-dielectric material and the second dielectric material.

2. The method of claim 1 wherein the spin-on-dielectric comprises silicon, nitrogen and hydrogen.

3. The method of claim 1 wherein the spin-on-dielectric consists essentially of silicon, nitrogen and hydrogen.

4. The method of claim 1 wherein the spin-on-dielectric comprises polysilazane.

5. The method of claim 4 wherein the second dielectric material comprises a doped silicon oxide.

6. The method of claim 4 wherein the second dielectric material comprises borophosphosilicate glass.

7. The method of claim 1 wherein the spin-on-dielectric consists essentially of polysilazane.

8. The method of claim 1 wherein the spin-on-dielectric consists of polysilazane.

9. The method of claim 8 further comprising, before forming the second dielectric material, densifying at least a portion of the polysilazane by exposing the at least a portion of the polysilazane to a temperature of from about 350°C to about 1000°C for a time of from about 15 minutes to about 2 hours.

10. The method of claim 9 wherein an entirety of the polysilazane is densified during the densifying.

11. The method of claim 9 wherein only a portion of the polysilazane is densified during the densifying.

12. The method of claim 11 wherein the polysilazane has a thickness and wherein less than or equal to 75% of the thickness is densified.

13. The method of claim 11 wherein the polysilazane has a thickness and wherein less than or equal to 50% of the thickness is densified.

14. The method of claim 1 wherein the polishing comprises chemical-mechanical polishing.

15. A method of forming a planarized surface over a semiconductor substrate, comprising:

providing a substrate comprising a memory array region and a peripheral region proximate the memory array region, the memory array region having a different average elevational height than the peripheral region;

forming polysilazane over the memory array region and over the peripheral region;

densifying at least a portion of the polysilazane;

forming a second material over the polysilazane, the second material having a different average elevational height over the memory array region than over the peripheral region; and

planarizing the second material while using the densified polysilazane as a stop, the planarizing utilizing conditions which remove the second material at a faster rate than the densified polysilazane, the planarizing forming a planarized surface which extends over the memory array and peripheral regions, the planarized surface comprising primarily the densified polysilazane over one of the memory array and peripheral regions and comprising primarily the second material over the other of the memory array and peripheral regions.

16. The method of claim 15 wherein a difference in the average elevational heights of the memory array and peripheral regions is from about 1000Å to about 3000Å.

17. The method of claim 15 wherein said one of the memory array or peripheral regions is the memory array region.

18. The method of claim 15 wherein the densifying occurs before the forming of the second material.

19. The method of claim 15 wherein an entirety of the polysilazane is densified during the densifying.

20. The method of claim 15 wherein only a portion of the polysilazane is densified during the densifying.

21. The method of claim 20 wherein the polysilazane has a thickness and wherein less than or equal to 75% of the thickness is densified.

22. The method of claim 20 wherein the polysilazane has a thickness and wherein less than or equal to 50% of the thickness is densified.

23. The method of claim 15 wherein the second material is an electrically insulative material.

24. The method of claim 15 wherein the second material comprises a doped silicon oxide.

25. The method of claim 15 wherein the second material comprises borophosphosilicate glass.

26. The method of claim 15 wherein the second material consists essentially of borophosphosilicate glass.

27. The method of claim 15 wherein the second material consists of borophosphosilicate glass.

28. A method of forming a planarized surface over a semiconductor substrate, comprising:

providing a substrate comprising a first region and a second region, the first region being a memory array region and the second region being peripheral to the memory array region, the first and second regions having first and second average elevational heights, respectively; the first average elevational height being greater than the second average elevational height;

forming a spin-on-dielectric material over the first and second regions of the substrate, the spin-on-dielectric material having a greater average elevational height over the first region than over the second region;

densifying at least a portion of the spin-on-dielectric material;

forming a second dielectric material over the spin-on-dielectric material, the second dielectric material having a greater average elevational height over the first region than over the second region; and

planarizing the second dielectric material while using the densified spin-dielectric material as a stop, the planarizing utilizing conditions which remove the second dielectric material at a faster rate than the densified spin-on-dielectric material, the planarizing forming a planarized surface which extends over the first and second regions of the semiconductor substrate, the planarized surface comprising primarily the densified spin-on-dielectric material over the first region of

the substrate and primarily the second dielectric material over the second region of the substrate.

29. The method of claim 28 wherein the densifying occurs before the forming of the second dielectric material.

30. The method of claim 28 wherein the spin-on-dielectric comprises polysilazane.

31. The method of claim 30 wherein the second dielectric material comprises a doped silicon oxide.

32. The method of claim 30 wherein the second dielectric material comprises borophosphosilicate glass.

33. The method of claim 28 wherein the spin-on-dielectric consists essentially of polysilazane.

34. The method of claim 28 wherein the spin-on-dielectric consists of polysilazane.

35. The method of claim 34 wherein the densifying comprises exposing the at least a portion of the polysilazane to a temperature of from about 350°C to about 1000°C for a time of from about 15 minutes to about 2 hours.

36. The method of claim 28 wherein an entirety of the polysilazane is densified during the densifying.

37. The method of claim 28 wherein only a portion of the polysilazane is densified during the densifying.

38. The method of claim 37 wherein the polysilazane has a thickness and wherein less than or equal to 75% of the thickness is densified.

39. The method of claim 37 wherein the polysilazane has a thickness and wherein less than or equal to 50% of the thickness is densified.